CORE MEMORY SENSE AMPLIFIER DESIGNS USING AN INTEGRATED DUAL COMPARATOR*

by R.J. Widlar

I. INTRODUCTION

A unique design for a core memory sense amplifier is described here. It uses a dual, differential voltage comparator rather than the usual differential amplifier, threshold-detector combination. The approach has the advantage of eliminating many of the tolerance problems encountered in the design of a sense amplifier.

Using the dual comparator, the sense amplifier threshold is determined by external resistors and is practically independent of integrated circuit characteristics. Excellent threshold stability over the full military temperature range is inherent in the design. Although operating at low power levels, the device is fast enough to work with 20-mil cores. Independent strobing of each comparator channel is provided, and pulse stretching on the output is easily accomplished. Up to eight sense amplifiers can be OR'ed directly. Finally, the output and strobing are compatible with practically all integrated logic forms.

II. DEVICE DESCRIPTION

Basically, the function of a comparator is to compare a signal voltage with a reference voltage and produce a digital one or zero at the output when one is higher than the other. The dual comparator described is two independent basic units with the outputs OR'ed. A strobe is provided on each side.

The operation of the comparator can be explained using the simplified schematic of a single side shown in Fig. 1. Since the comparator is expected to detect when the voltage on the two input terminals is equal, a differential input stage (Q_1 and Q_2) is used so that the emitter base voltages cancel when the input is zero. The emitters of the input stage are supplied from a current source (Q_{11}) to make their collector current insensitive to the common mode input voltage. A balanced second stage is also used: Q_4 is the actual second stage amplifier while Q_3 provides balanced biasing for Q_4. The second stage can be understood by considering that Q_3 and Q_4 are identical transistors. Their bases are fed from a common voltage point through identical resistors (R_1 and R_2). When the input stage collector currents are equal, the collector currents of Q_3 and Q_4 will be equal, so the second stage is balanced. Q_3 also functions as a unity gain amplifier which inverts the output of Q_1 and combines it with the output of Q_2 at the base of Q_4. A single-ended output is obtained at the collector of Q_4. One feature of the second stage is that under balanced conditions the single-ended output is insensitive to changes in positive supply voltage. If the positive supply voltage is increased, the collector currents of both Q_3 and Q_4 will increase such that the voltage on the collector of Q_4 remains constant.

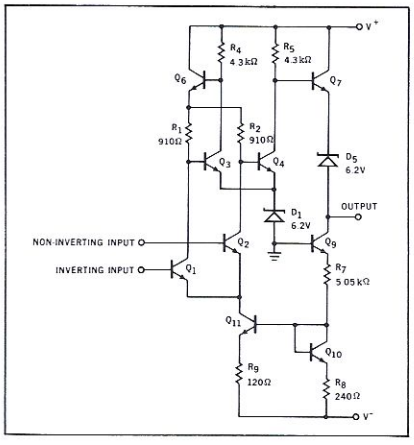

Fig. 1. Simplified schematic of half the dual comparator.

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An emitter follower is used at the output of Q_4 to give a high output current capability. A zener diode (D_1) in the emitters of the second stage transistors provides a large input voltage range (the positive input voltage limit is essentially equal to the voltage on the base of the second stage transistors). An identical zener diode in the output emitter follower (D_5) level shifts the output back to a level compatible with logic circuits. Q_9 isolates the output from the diode compensated bias divider for the input stage current source. Using the diode connected transistor, Q_{10}, to compensate for the emitter-base voltage of Q_{11} permits the current source to operate with a small voltage drop across its emitter resistor, R_9. This gives an increased negative common mode limit.

As can be seen from the complete schematic in Fig. 3, there is an additional transistor, Q_5. The purpose of this transistor is to reduce the base drive on Q_4 when it saturates. This action not only gives a lower power dissipation but also reduces the storage time of Q_4.

When the comparator is operating in the active region, the collector current of Q_2 produces a voltage drop across R_6 which keeps Q_5 in a nonconducting state. Hence, Q_5 does not influence operation in the active region. With a large negative input, Q_2 is turned off and no longer produces this hold-off voltage across R_6, so R_5 conducts. Q_5 can conduct the entire current through R_4 with only a small voltage drop across R_2 and R_6. R_1 has a large voltage drop across it since the collector current of Q_1, which is nearly the entire collector current of Q_{11}, is flowing through it. This voltage drop across R_1 cuts off Q_3. This state of operation, with Q_5 conducting and Q_3 cut off, is illustrated in the simplified schematic of Fig. 2. R_6 is eliminated since the voltage drop across it is small enough to be neglected.

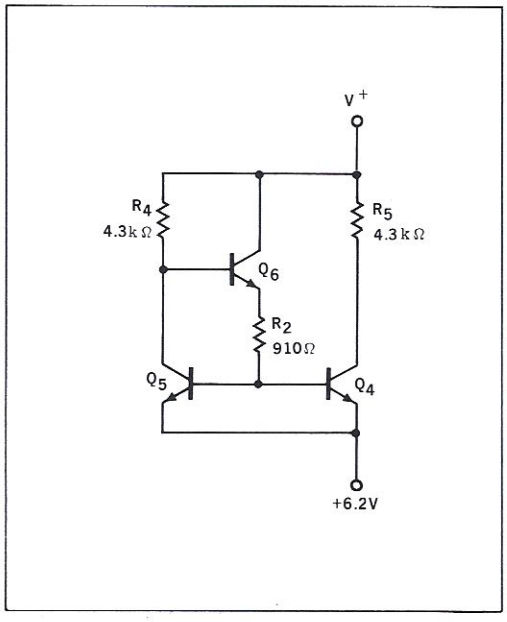

Fig. 2. Simplified schematic showing operation of the saturation limiter circuitry.

If it is assumed that Q_4 and Q_5 in Fig. 2 are identical transistors, their collector currents will be equal since they are operating with the same emitter-base voltage. The collector current of Q_5 is determined by R_4 and the voltage drop across it. The collector-to-emitter voltage of Q_5 will be two emitter-base voltage drops (Q_5 and Q_6) plus the voltage drop across R_2, which is small. The collector-to-emitter voltage of Q_4 will be equal to that of Q_5 since their collector currents are equal and R_5 is equal to R_4. However, it is desired that Q_4 saturate in order to get the proper negative output level. This can be accomplished by making the emitter junction of Q_5 smaller than that of Q_4, so that Q_4 will conduct more current than Q_5 with the same emitter-base voltage (this is easily accomplished in a monolithic integrated circuit). With the proper ratio of device geometries, Q_4 can be made to go just barely into saturation, giving a minimum storage time.

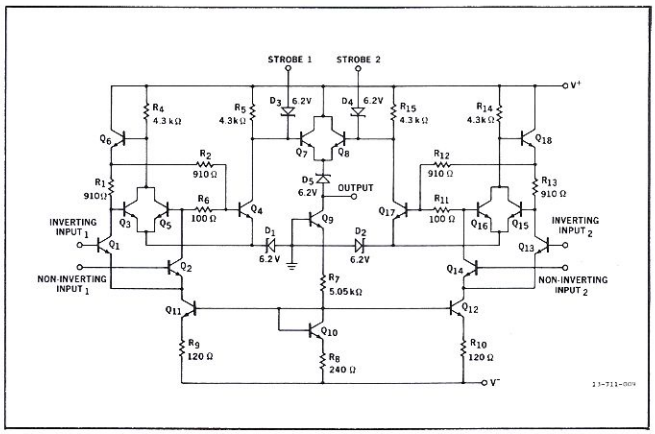

Fig. 3. Complete schematic of the Fairchild μA711 dual comparator.

With the dual comparator in Fig. 3, the individual comparators are OR'ed at the emitters of the output emitter followers. Only a single level shifting zener diode and bias divider are used. Zener diodes on the bases of the output emitter followers provide independent strobing on each channel: when the strobe on one side is held down to ground level, the output of that side cannot rise. The strobe terminal can also be used to clamp the positive output swing since the output voltage will always be at least one diode drop less than the voltage on the strobe terminal.

A mathematical analysis of the comparator operation is given in Ref. 1. It is shown that circuit performance is not affected by the loose component tolerances encountered with monolithic construction but depends on how well various parts match—something which is easily done in an integrated circuit. Since this matching can be maintained well over an extremely wide temperature range, the comparator is relatively insensitive to changes in operating temperature. In addition, it is demonstrated in the reference that the comparator is not greatly affected by supply voltage variations over a wide range. The only significant parameter variation is voltage gain, but this is reduced to a second-order term in normal applications.

III. DEVICE PERFORMANCE

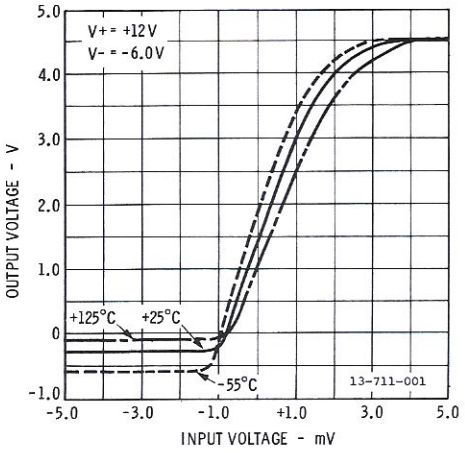

Fig. 4. Voltage transfer characteristic.

The transfer function of the comparator at various operating temperatures is illustrated in Fig. 4. This proves that the performance is not greatly affected by temperature. The fact that gain increases at low temperatures and decreases at high temperatures indicates that the circuit is dependent on the highly predictable transconductance of the transistors rather than current gain. It is also worthwhile to note that the comparator is not designed to have zero output for zero input as is an operational amplifier. Instead, it has an output offset voltage equal to the threshold voltage of common integrated logic circuits. This output offset voltage also has approximately the same temperature coefficient as the threshold of the logic. The fact that the output offset voltage of the comparator matches the logic allows a lower gain with no loss in over-all accuracy and permits the gain of the logic circuit to be added to the gain of the comparator in determining over-all resolution (this gives an equivalent gain of 50,000 with Fairchild DTL). This is important since additional gain stages would not only complicate the comparator but also would make it slower.

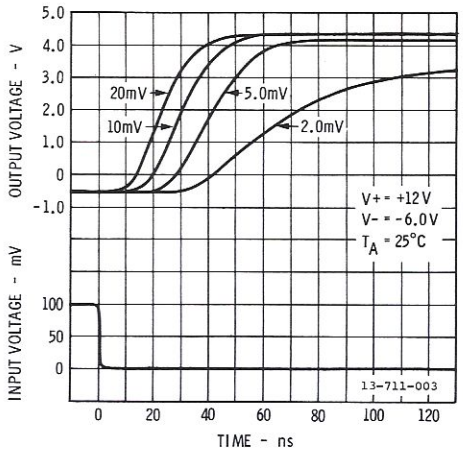

Fig. 5. Response time for various input overdrives.

The response time is shown in Fig. 5. The response time is defined as the interval between the application of an input step function and the time when the output crosses the threshold voltage of the logic. The input step drives the comparator from some initial, saturated input voltage to an input level just barely in excess of that required to bring the output from saturation to the logic threshold voltage. The excess is referred to as the voltage overdrive. This definition eliminates offset voltage from the speed measurement in order to provide more flexibility in the interpretation of specified parameters. In Fig. 5, the input step height is 100 mV and overdrives of 2 mV, 5 mV, 10 mV, and 20 mV are shown. The response times are 65 ns, 40 ns, 28 ns, and 20 ns respectively for these overdrives. For smaller input steps, the response time will be somewhat faster for the same overdrive since the internal circuitry of the comparator will not be completely saturated before the pulse is applied. Larger input steps do not materially affect response time since the comparator does not go any deeper into saturation with input voltages larger than 100 mV. Measurement of response time in the manner stated above permits a determination of how much input-referred error is encountered when the comparison is made in a short time interval.

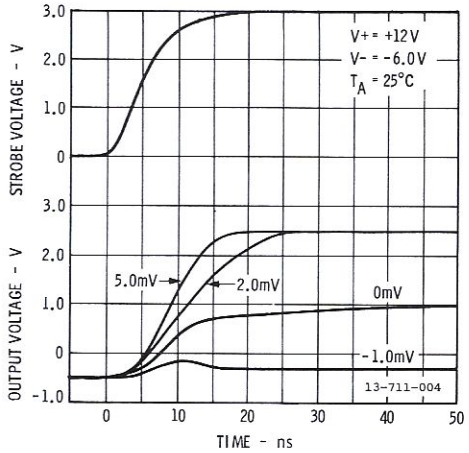

Fig. 6. Strobe release time for various input overdrives.

The speed of the strobe circuitry is indicated in Fig. 6. The strobe release time is the time required for the output to rise to the logic threshold voltage after the strobe terminal has been driven from the zero to the one logic level. The strobe release time is shown for various input conditions in the figure. The 0 mV curve is for an input condition which would put the output at the logic threshold voltage under d-c conditions. The curve below that is for 1 mV less input voltage and gives an indication of the feed-through of the strobe pulse when the comparator is barely turned off (it is necessary to wire the comparator into the circuit minimizing the stray capacitance between the strobe terminal and the inputs in order to keep this feed-through small). The 2 mV and 5 mV curves represent actual operating conditions and give strobe release times of 14 ns and 10 ns respectively. In these curves, the output does not rise to the maximum output level because of the clamping action of the strobe circuitry when a low amplitude strobe pulse is used. The test conditions shown are representative of the case where the comparator is used with Fairchild RTL.

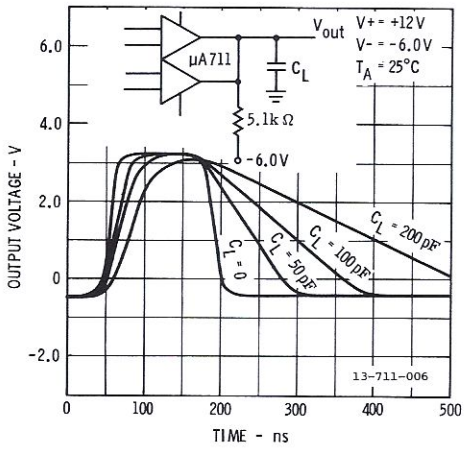

Fig. 7. Output pulse stretching with capacitive loading.

Frequently in the design of a sense amplifier where time strobing is used, it becomes necessary to stretch the strobed output pulse of the sense amplifier in order to make it wide enough to be transmitted over a reasonable line length and trigger the storage circuits. The most straightforward way of accomplishing this is to use a one-shot multivibrator. However, the accuracy requirements for the stretched pulse do not warrant going to the complexity of a one-shot. Much simpler methods can be used. Figure 7 shows a possible alternative. Loading the comparator with a capacitor on the output will stretch the output pulse. This occurs because the output emitter follower can charge the load capacitance rapidly, but the output current sink gives a limited rate of discharge. Normally, the strobe width is enough to trigger the logic circuits. and the only fear is that the pulse will be degraded by cable capacitance. However, with the μA 711, the capacitances encountered in transmission make the output pulse longer rather than shorter so no discrete capacitor need be used. In the test circuit for Fig. 7, and external resistor is connected between the output and the negative supply to give the μA 711 a fan-out of one with DTL. This gives considerably less pulse stretching than would be seen with the μA 711 alone. It is worthwhile to point out here that the response time and the strobe release time for negative-going outputs were not described previously because they are limited by this pulse stretching characteristic. The negative-going response time up to the base of the output emitter follower is faster than the positive-going response time because the storage time of the second stage amplifier is not involved. Similarly, the strobe pull-down time is shorter than the release time on the base of the output emitter follower since a negative-going strobe pulse into the zener diode will forcibly pull down that point. Therefore, the negative-going response times are limited more by the characteristics of the load than by those of the circuit and are described by Fig. 7.

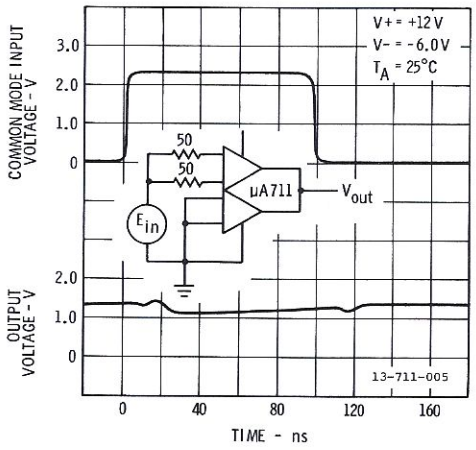

Fig. 8. Common mode pulse response.

The d-c common mode rejection of the μA 711 is typically 85 dB. This is considerably more than can be used in a practical high-speed circuit so it is of little interest. What is of much more significance is the common mode rejection at high frequencies. If this is expressed in terms commonly used in connection with differential amplifiers, it is difficult to interpret for a comparator. However, Fig. 8 shows a pulse test and its result which demonstrates that the comparator is affected little by fast common mode signals even in the center of its active region. That is, the error encountered due to any reasonable high-frequency, common mode signals present during comparison is small with respect to the offset voltage and speed resolution. At any time other than when the comparison is being made, common mode signals can be completely neglected.

The over-all performance of the μA 711 is summarized in Table I. The low offset and thermal drift is proof of the inherent balance of the circuit and the benefit of monolithic construction.

TABLE I

TYPICAL PERFORMANCE OF THE μA 711 COMPARATOR

Conditions: $T_A = 25°C$, $V^+ = 12.0\,V$, $V^- = -6.0\,V$

Input Offset Voltage	1 mV
Input Offset Current	0.5 μA
Input Bias Current	25 μA
Temperature Coefficient of Input Offset Voltage	3 μV/°C
Input Voltage Range	± 5.0 V
Voltage Gain	1500
Response Time	40 ns
Strobe Release Time	12 ns
Output Resistance	200 Ω
Positive Output Level	+4.5 V
Negative Output Level	-0.5 V
Power Consumption	130 mW

IV. LOGIC COMPATIBILITY

The output of the μA 711 is designed to be compatible with all integrated logic forms. However, because of the substantial differences in the many kinds of logic, it is obvious that the same loading rules used for all these logic families cannot be directly applied to the comparator. Some compromises must be made. In what follows, some of these considerations are discussed.

The output of the dual comparator is designed such that a number of them can be wire OR'ed as is often required in memories. Up to eight devices can be OR'ed, yet the output levels will still be compatible with Fairchild RTL, DTL, and T^2L for a fan-out of two.

In order to make possible this OR'ing capability and hold the device dissipation to levels satisfactory for operation over the full military temperature range, it was necessary to reduce the sink current of the comparator. As a result, at least four devices must be OR'ed before they can provide enough sink current for a DTL fan-out of one. If a single comparator is used to drive a DTL circuit, a 5.6 kΩ resistor must be inserted between the output terminal and the -6 V supply for a worst-case fan-out of one. For a fan-out of two, a 2.4 kΩ resistor must be used.

With standard Micrologic® IC's, a single μA 711 can handle a fan-out greater than eight. However, even with a fan-out of one, the comparator should not be operated continuously in the positive output state because of excessive power dissipation from the resulting large output current. In the sense amplifier application, this is not a problem because of the low duty cycle of the positive output condition. However, this excessive output current does increase the storage time of the Micrologic. This can be prevented by inserting a resistor in series with the comparator output. Maximum values for this resistor would be 3.9 kΩ for a worst-case fan-out of one, 1.8 kΩ for a fan-out of two, and 820 Ω for a fan-out of three. A small capacitor can be put across this limiting resistor to increase the speed of the logic. If a number of comparators are wire OR'ed, this limiting resistor should be reduced somewhat to compensate for the lower positive output level of the comparator.

The current normally required by the μA 711 to strobe down one of the outputs is 1.2 mA. However, if the comparator is in a nondisturbed state, no current is required from the strobe-driving logic since the second stage of the comparator is supplying the current. When a number of comparators are used as sense amplifiers and are strobed on a common line, only one side of one comparator is likely to be disturbed at any one time. Therefore, it is not necessary that the strobe logic circuitry be able to sink the worst-case current for all the comparators it is driving. As a matter of fact, it is only required that the strobe circuitry be able to sink the worst-case current for one side of one of the comparators.

V. SENSE AMPLIFIER CIRCUITS

Conventional sense amplifiers are usually differential-input, differential-output amplifiers which amplify the output of the cores and eliminate the comparatively large common mode signals present during read. A full-wave rectifier and sense-level threshold are inserted at the output of the amplifier to discriminate between the zero and one outputs of the cores.

This approach has the disadvantage that the offset voltage, the differential gain, the output common mode level, the rectifier offset, and the output threshold level must all be accurately controlled to get a precise input-referred threshold level. A much more satisfactory solution is to use a voltage comparator and insert the threshold voltage at the input. In this case, the accuracy is only affected by the offset voltage of the comparator (which similarly affects the differential amplifier in the conventional approach). Variations in voltage gain and frequency response do not affect accuracy as long as these are high enough.

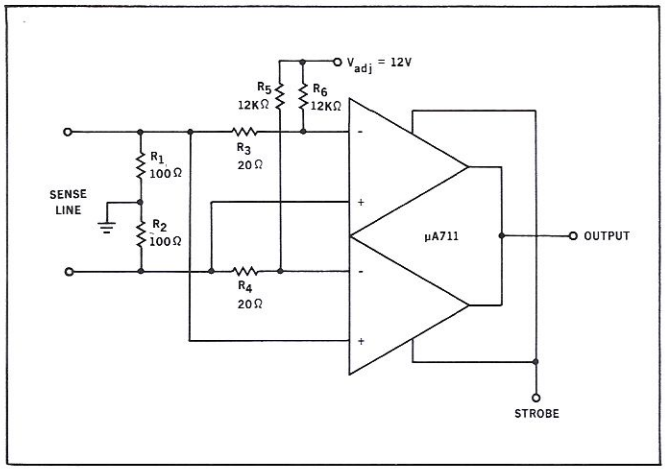

Fig. 9. Basic sense amplifier configuration.

The problem in using a voltage comparator as a sense amplifier has been that the threshold voltage is not easily inserted at the input when common mode rejection is required. A straightforward approach to the problem requires a floating voltage source. However, the circuit in Fig. 9 inserts the threshold at the input using a grounded supply, yet it provides respectable common mode rejection. In the circuit, R_1 and R_2 provide termination for the sense line. The sense level is essentially equal to the voltage across R_3 and R_4 caused by the current from the positive supply (V_{adj}) through R_5 and R_6. The grounded tap on the line termination resistors provides a sink for this current. The use of two comparators enables the circuit to respond to either positive or negative input signals above the preset threshold.

The advantages of this approach using the dual comparator are many. It does not require anything that is difficult to do in the integrated circuit, which means that it can be produced and delivered. Further, the threshold level is determined by inexpensive external resistors so a single dual comparator design can be used for a wide variety of core sizes. This permits standardization and allows production volumes that make use of the true economies of integrated circuits. The threshold voltage can also be easily adjusted to match the optimum value for a particular memory bank. This is done with a single adjustment for the entire battery of sense amplifiers by varying V_{adj}. In addition, because only input offset voltage is the prime determinant of threshold inaccuracy, the change of threshold voltage with temperature can be held to a minimum. This is important even though core outputs vary substantially with ambient temperature for a constant current drive. The reason is that if write and read functions are to be done at different temperatures, the core variation must be compensated with the current drive for the cores. If an attempt is made to compensate for core thermal variations with corresponding thermal changes in sense amplifier threshold, it is not practical to write into the cores at one temperature and read out at another. The best situation is for the sense amplifier to maintain a constant threshold over the full temperature range.

With the circuit in Fig. 9, the sense level will be affected by a common mode signal, although only by approximately 8 percent for a one-volt signal with V_{adj} = 12 V. This is rarely a problem because the common mode signal during read is less than 0.5 V in most memories. This sensitivity can be reduced by increasing R_5 and R_6 and using a higher voltage to set the threshold. In the unusual case where very large common mode signals are present during read, the circuit in Fig. 10 can be used. This circuit uses additional resistors to balance the input bias network to the common mode signal, and it provides at least an order of magnitude better common mode rejection. This circuit is especially useful if the resistor network is purchased as a thin (or thick) film assembly since the extra resistors add little complexity to the complete assembly and since the tolerance on the balancing resistors can be looser than the tolerance on the threshold-determining resistors.

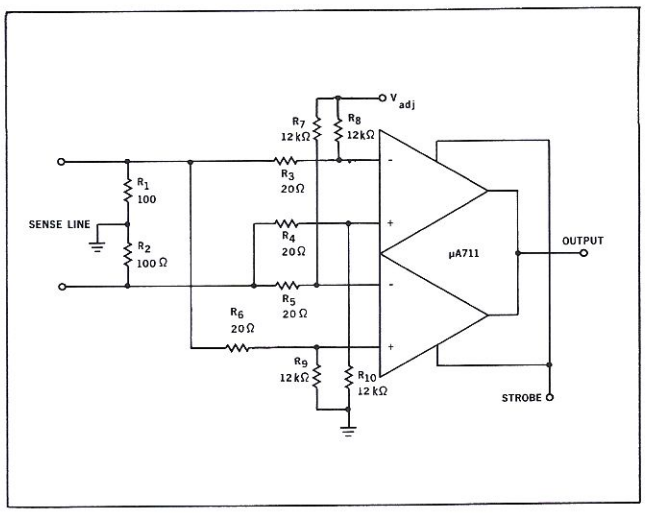

Fig. 10. Sense amplifier with improved insensitivity to common mode signals.

The high-frequency common mode rejection can be severely degraded by unbalanced stray capacitances on the sense line and on the comparator input. For this reason, low-capacitance resistors should be used for R_5 and R_6; the physical layout should also be such as to minimize strays.

Because the comparator is directly coupled and employs low storage time devices, the recovery from either differential or common mode overloads is less than 50 ns regardless

of their amplitude. The direct coupling also removes the pattern sensitivity of threshold voltage seen with a-c coupled amplifiers.

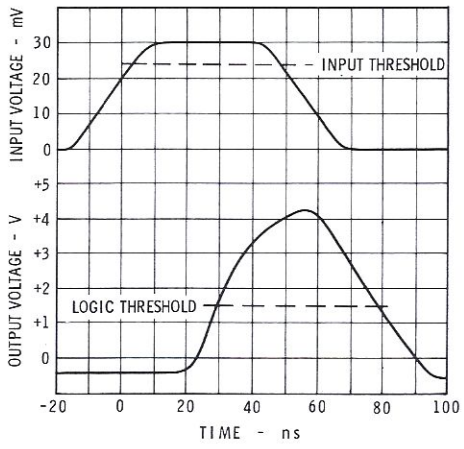

Fig. 11. Response of the basic sense amplifier circuit, with a 23 mV threshold setting to a 30 mV input pulse.

The response of the sense amplifier to a typical input one is shown in Fig. 11. With an input signal that is 7 mV above the discrimination level for 45 ns, an output pulse that is above the logic threshold for 50 ns is obtained. Longer output pulses can be obtained using the pulse stretching techniques described earlier.

In determining the recovery time of the sense amplifier to an overload or to a maximum zero when time strobing is used, only the response time of the input stage need be considered. This is true because the second stage is held in saturation by the strobe. Hence, when the amplifier is recovering from the input signal, the feedback capacitance of the second stage does not slow the recovery. Since the

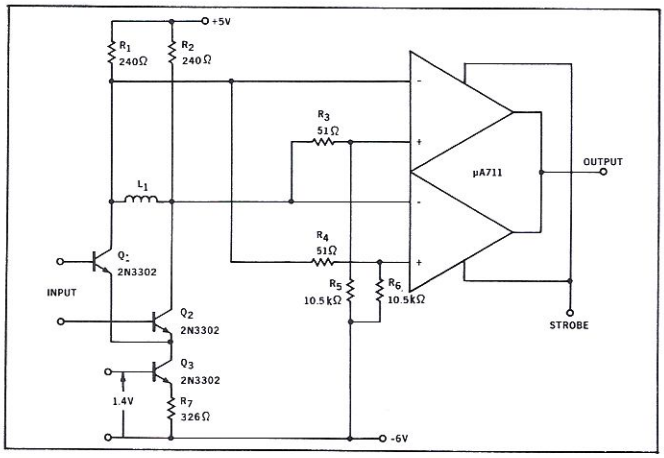

Fig. 12. Sense amplifier circuit using temperature compensated preamplifier for increased threshold sensitivity.

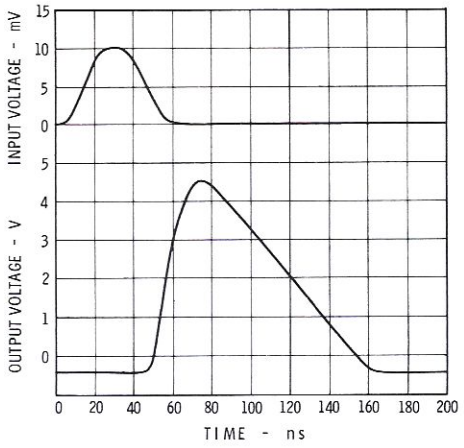

Fig. 12b. Response to 10 mV input pulse for 5 mV threshold.

over-all response time of the device is limited by this feedback capacitance (and second stage storage), recovery is exceptionally fast; the strobe signal can therefore be applied almost immediately after the input signal goes below the input discrimination level without obtaining a false output.

When working with very small cores, the output signal can be so small as to approach the offset of the comparator. In this case, some sort of amplification is required before going into the sense amplifier. In addition, since d-c offset will be a basic limitation on discrimination level in the preamplifier stage, a-c coupling is also required. A method of accomplishing this is shown in Fig. 12. A differential input stage is used as a preamplifier with a gain of 10. Its output is coupled into the dual comparator connected as a sense amplifier, with a threshold voltage setting of 50 mV, in a circuit similar to that in Fig. 9. An inductor (L_1) is used to remove the offset of the input stage transistors so a matched pair does not have to be used. The differential preamplifier achieves temperature compensated operation, within a few percent, over the entire -55°C to +125°C temperature range without the use of emitter degeneration resistors. This is an advantage since the degeneration resistors deteriorate common mode rejection and give non-optimum high frequency characteristics. Conditions for achieving this compensated operation independent of the individual transistor characteristics are derived in Appendix A. The gain of the preamplifier, and therefore the equivalent input-referred threshold voltage, is most conveniently set by adjusting R_7.

With the circuit as shown in Fig. 12, the sense threshold is 5 mV. Both the input stage and the dual comparator circuit provide common mode rejection. The response of the sense amplifier to a 10 mV input signal is shown in Fig. 12b; this can be improved by operating the preamplifier stage at a higher current than the nominal 1 mA in the indicated design.

A number of sense lines can be combined into a single sense amplifier using a circuit similar to that in Fig. 12. Individual differential amplifiers and compensated current sources are used for each sense line. These differential amplifiers are combined into a single set of load resistors. If more than two, or possibly three, differential amplifiers are used, the inductor, L_1, should be removed, and a pair of inductors should be connected across the load resistors, R_1 and R_2, to prevent excessive d-c voltage drop across them.

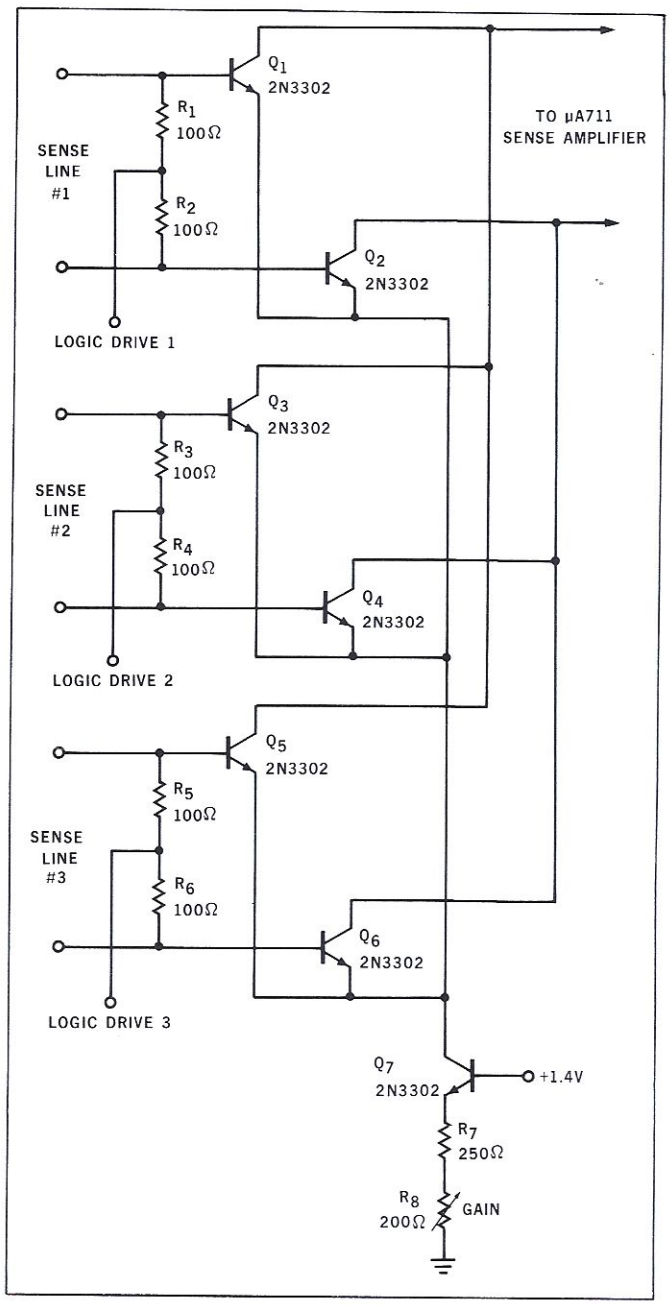

Fig. 13. Three-channel gated preamplifier for sense amplifier.

In certain instances it is convenient in the design of a memory to gate a number of sense lines into a single sense amplifier. A circuit which accomplishes this is shown in Fig. 13. Differential preamplifiers are employed on each sense line. These are operated from a single temperature-compensated current source. The digital gate signal is applied to the center tap on the line termination resistors. The differential pair that has the highest input common mode signal will operate while the remainder will be cut off since their emitter-base junctions will be reverse-biased. The common-collector outputs of the preamplifiers are fed to a μA711 connected as a sense amplifier as shown in Fig. 12.

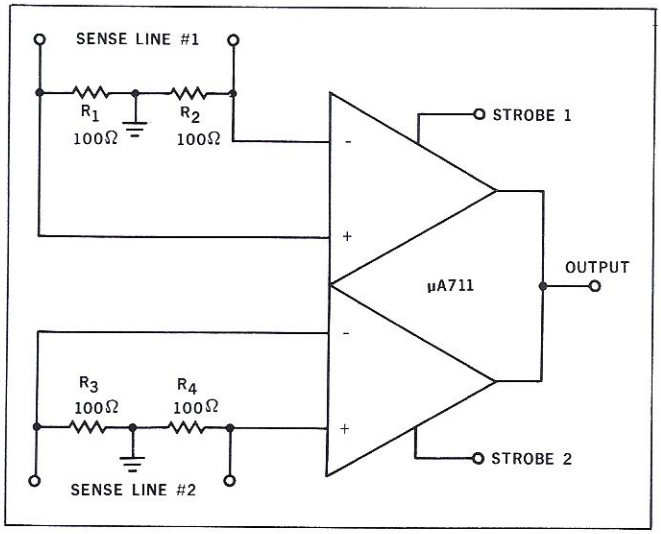

Fig. 14. Dual sense amplifier for positive-one, negative-zero memory systems.

If the inductor in Fig. 12 is used with the front end in Fig. 14, the circuit should be gated on for a time that is long by comparison to the time constant of the inductor and the collector load resistors before trying to read. This is required for the collector current imbalance—caused by offset between the differential transistors—to settle out. The inductor, however, can be eliminated if matched input transistors (2N3729) are used and if the offset of the input transistors is small by comparison to the desired threshold.

The logic drive circuitry should present a low impedance to the center tap on the line termination resistors so that an excessive common mode signal is not developed. The gain of the preamplifiers and, therefore, the threshold setting are best adjusted by varying the emitter resistance in the current source as shown in Fig. 13.

Certain types of memories (i. e., biax or nondestructive read) give an output of one polarity for a one and an output of the opposite polarity for a zero. In these applications, one-half the μA711 can be used as a sense amplifier. No resistor network need be employed on the input to determine threshold

since the comparator alone is designed to detect zero crossing. The complete μA 711 can be used as a dual sense amplifier with common outputs. The outputs can be separated as far as the system logic is concerned by using the independent strobe terminals. A circuit for this is shown in Fig. 14.

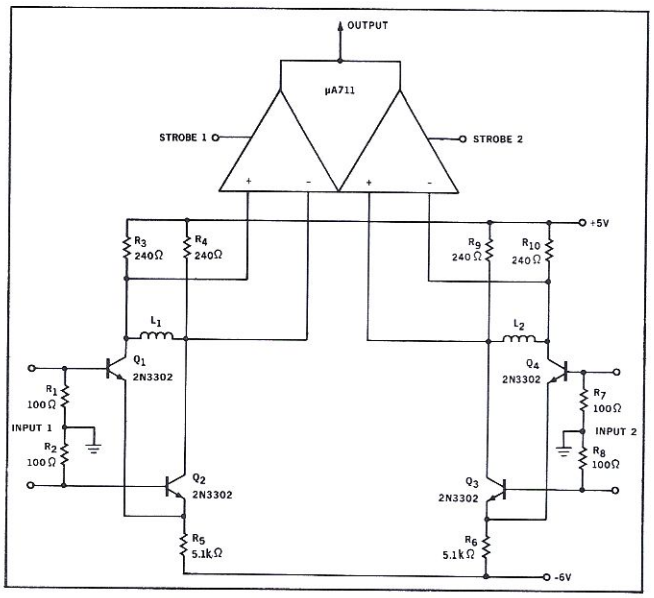

Fig. 15. Dual sense amplifier for positive-one, negative-zero memory systems including preamplifiers.

Most often with positive one, negative zero memories, the output pulse amplitude is comparable to the offset of the μA 711. In this case, the circuit in Fig. 14 cannot be used alone. A preamplifier with a-c coupling must be used to amplify the signal to a level that can be discriminated reliably by the μA 711. A circuit for doing this is shown in Fig. 15. It is similar to the preamplifier in Fig. 12 except that no attempt is made to control accurately the gain since its actual magnitude is unimportant as long as it is high enough. As with the circuit in Fig. 12, the inductors remove the offset of the preamplifier transistors so matched pairs do not have to be used. The preamplifier shown has a gain of ten, so the circuit will be able to discriminate a zero crossing within 0.5 mV.

In many military systems, it is desirable to hold the sense amplifier dissipation to a minimum either to lower power consumption or because of heat removal problems associated with high packing densities. If this is the case, power supply strobing can be used with the μA 711 to reduce power consumption from the typical 130 mW to about 40 mW per package. A circuit for doing this is shown in Fig. 16. The positive supply voltage is strobed from +5 V in the non-operating state to +12 V for operation. With +5 V and -6 V supply voltages, the input and output stages of the comparator function in the normal manner (for zero output), and only the second stage is affected. As a result, neither the sense lines nor the logic circuits on the output are disturbed by lowering the positive supply. When the positive supply is applied, the sense amplifier stabilizes within 30 ns and no perturbations are sent out on the sense line, so it is ready to function within this time. The supply strobing must be employed along with the strobe on the usual terminal because a feedthrough pulse of approximately 10 ns width will come through the sense amplifier even with an input zero if the output strobe terminal is not held down. Normally, the supplies can be strobed along with the core drivers and the output strobe terminal can be driven after the usual delay required for the sense line to settle down.

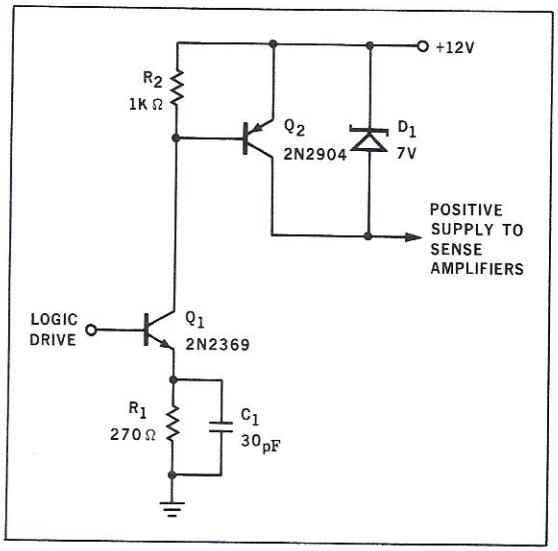

Fig. 16. Positive-supply strobe circuit.

The circuit in Fig. 16 provides a simple way of accomplishing supply strobing. This circuit is capable of driving at least ten sense amplifiers. With a logic zero input to Q_1, Q_2 is cut off and the zener diode determines the low-state, positive input to the sense amplifiers. When the logic signal is applied, Q_1 turns on, applying full voltage to the circuits. The speed-up capacitor, C_1, assists in rapid turn-on. The turn-off is not too rapid because of the storage time of Q_2, but this is usually of little significance because the sense amplifier can be quieted by using the output strobe terminal.

VI. CONCLUSION

A unique design for a core memory sense amplifier using an integrated dual comparator was described. The method gives unusual precision and reliability yet requires

from the integrated circuit only what can be done consistently at low cost—thus assuring availability. With this approach, a single integrated circuit can be used as a sense amplifier for practically all coincident current cores presently used. In addition, the circuit is ideally suited to such positive one, negative zero memories as biax and nondestructive read. In most applications, the dual comparator can be used with only an external resistor network to determine threshold; for very demanding applications, the dual comparator can be combined with relatively inexpensive discrete parts to obtain the required performance.

The design of the dual comparator makes use of the excellent matching and low wiring capacitances available with monolithic construction. The device has exceptionally stable d-c characteristics over a wide temperature range and response times superior to discrete component circuits of comparable performance and power dissipation. The circuit is also very tolerant to normal variations in supply voltages. Its simplicity and suitability for integration is demonstrated by the fact that it is constructed on a 40-mil-square die using a Planar* epitaxial process almost identical to that used for common digital integrated circuits. A photomicrograph of the circuit is shown in Fig. 17.

*Planar is a Fairchild-patented process.

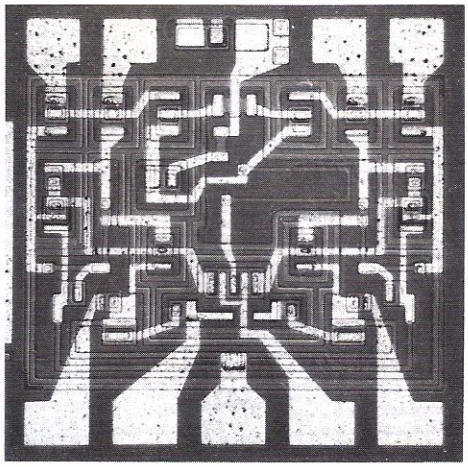

Fig. 17. Photomicrograph of the μA711 dual comparator.

VII. REFERENCES

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2. A. J. W. M. van Overbeek, "Tunable Resonant Circuits Suitable for Integration," 1965 International Solid State Circuits Conference Digest of Technical Papers, Vol. VIII, p. 92.

3. R. D. Thornton, D. deWitt, E. R. Chenette, and H. C. Lin, "Characteristics and Limitations of Transistors," John Wiley and Sons, Inc., New York, N.Y., Note 1, S.E.E.C., 1963.

APPENDIX A

DIFFERENTIAL AMPLIFIER TEMPERATURE COMPENSATION

It is pointed out in Ref. 2 that the voltage gain of the differential amplifier configuration shown in Fig. 1A can be made insensitive to temperature over the operating range of the transistors by choosing a suitable bias voltage, V_B. The derivation giving conditions for this compensation will be presented here and the differences between practical transistors and the theoretical model will be evaluated.

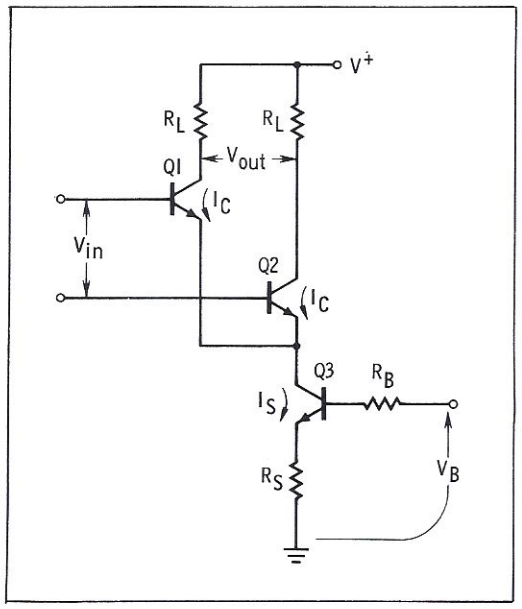

Fig. 1a. Differential input stage configuration.

Reference 3 shows that the collector current of a transistor can be expressed as

$$I_C \cong \alpha T^n \exp\left[\left(V_{BE} - V_{g0}\right)\frac{q}{kT}\right] \qquad (1)$$

where α and n are constants that depend on how the transistor is made, T is absolute temperature, V_{BE} is the base-emitter voltage, V_{g0} is the extrapolated energy gap for the semiconductor material at absolute zero, q is the charge of an electron and k is Boltzmann's constant. The expression is valid for $V_{BE} > 4kT/q$, up to high currents where emitter contact and base spreading resistances become important and down to low currents where collector leakage currents cause inaccuracy. The equation is not dependent on the transistor current gains, except for the influence on the constant, α.

Differentiating Eq. (1) with respect to V_{BE} yields

$$\frac{\partial I_C}{\partial V_{BE}} = \frac{qI_C}{kT}, \qquad (2)$$

which is the transconductance of the transistor.

The differential gain of the amplifier in Fig. 1A is given by

$$A_V = \frac{dV_{OUT}}{dV_{IN}} = \frac{\partial I_C}{\partial V_{BE}} R_L = \frac{qR_L I_C}{kT} \qquad (3)$$

But for very large current gain in Q_1 and Q_2, $I_C = I_S/2$, so we have

$$A_V = \frac{qR_L I_S}{2kT} \qquad (4)$$

It is desired that $\partial A_V/\partial T = 0$. Differentiating (4) we find that

$$\frac{\partial A_V}{\partial T} = \frac{qR_L}{2kT}\left[\frac{\partial I_S}{\partial T} - \frac{I_S}{T}\right] \qquad (5)$$

If in the circuit of Fig. 1A a very large current gain for Q_3 is assumed, the current source current is given by

$$I_S = \frac{V_B - V_{BE}}{R_S} \qquad (6)$$

Hence, solving for V_{BE}, we can write

$$V_{BE} = V_B - I_S R_S \tag{7}$$

Substituting this for V_{BE} in Eq. (1) gives us

$$I_S = \alpha T^n \exp\left[\left(V_B - I_S R_S - V_{g0}\right)\frac{q}{kT}\right] \tag{8}$$

Further, differentiation of Eq. (8) yields

$$\frac{\partial I_S}{\partial T} = \frac{I_S}{T}\left[\frac{V_{g0} + \frac{nkT}{q} - V_B + I_C R_S}{\frac{kT}{q} + I_C R_S}\right] \tag{9}$$

Substituting into Eq. (5), the result is

$$\frac{\partial A_V}{\partial T} = \frac{qR_L I_S}{2kT^2}\left[\frac{\frac{kT}{q}(n-1) - V_B + V_{g0}}{\frac{kT}{q} + I_C R_S}\right] \tag{10}$$

which is equal to zero for

$$V_B = V_{g0} + (n-1)\frac{kT}{q} \tag{11}$$

The extrapolated energy gap (V_{g0}) for silicon is 1.205 V, the constant n has a typical value of 1.5 for NPN silicon transistors and kT/q = 25.8 mV at room temperature. Hence, using V_B = 1.218 V gives a temperature-drift error less than one percent over a -55°C to +125°C temperature range.

The above analysis made a number of assumptions about the transistors used in the circuit. By far, the most significant terms that cause deviation from the result obtained in Eq. (11) are the finite current gains of the transistors and the nonzero emitter and base resistances in the differential pair. The influence of these second-order terms will now be considered. The analysis is an extension of the bisectional theorem and makes the approximation that the interaction between these second order terms is negligible.

If the current gain of Q_3 is taken into account, we find that

$$I_S \cong \frac{V_B - \frac{I_S R_B}{h_{FE}} - V_{BE}}{R_S} - \frac{I_S}{h_{FE}}$$

$$= I_{SO} - I_{SO}\left[\frac{R_B}{R_S h_{FE}} - \frac{1}{h_{FE}}\right] \tag{12}$$

where $I_S R_B/h_{FE}$ is the drop across the bias-source resistance from the base current of Q_3 and I_S/h_{FE} represents the difference in the emitter and collector currents of Q_3.

Similarly, the collector current of the differential stage is

$$I_C = \frac{I_S}{2} - \frac{I_C}{h_{FE}} \tag{13}$$

Using the fact that $I_C \cong I_{SO}/2$ and combining with Eq. (12) gives

$$I_C = \frac{I_{SO}}{2}\left[1 - \frac{R_B}{R_S h_{FE}} - \frac{2}{h_{FE}}\right] \tag{14}$$

Substituting into Eq. (3),

$$A_V = \frac{qR_L I_{SO}}{2kT}\left[1 - \frac{R_B}{R_S h_{FE}} - \frac{2}{h_{FE}}\right] \tag{15}$$

or from Eq. (4)

$$A_V = A_{VO}\left[1 - \frac{R_B}{R_S h_{FE}} - \frac{2}{h_{FE}}\right] \tag{16}$$

Therefore,

$$\Delta A_V = A_V - A_{VO}$$

$$= -\frac{A_{VO}}{h_{FE}}\left(\frac{R_B}{R_S} + 2\right) \tag{17}$$

which is the change in voltage gain for finite current gain.

The emitter contact and base spreading resistances will now be taken into account. Base spreading resistance can be eliminated either by operating the transistors at sufficiently low collector currents or by choosing a suitable transistor with a stripe geometry for higher current operation. Hence, only emitter contact resistance need be considered. Including the effect of emitter contact resistance in Eq. (4) yields

$$A_V = \frac{R_L}{\frac{2kT}{qI_S} + R_E} \tag{18}$$

so that

$$\frac{\partial A_V}{\partial R_E} = -\frac{R_L}{\left(\frac{2kT}{qI_S} + R_E\right)^2}$$

Since $R_E << \frac{qI_S}{2kT}$, we have

$$\frac{\partial A_V}{\partial R_E} = -\left(\frac{qI_S}{2kT}\right)^2 R_L \tag{19}$$

which, using Eq. (4), becomes

$$\frac{\partial A_V}{\partial R_E} = \frac{A_{VO}^2}{R_L}$$

With a few arguments, this can be written as

$$\Delta A_V = \frac{A_{VO}^2 \, \Delta R_E}{R_L} \tag{20}$$

Because the initial (ideal) value of R_E is zero, Eq. (20) becomes

$$\Delta A_V = \frac{A_{VO}^2 \, R_E}{R_L} \tag{21}$$

which is the change in voltage gain due to nonzero emitter contact resistance.

The change in voltage gain with changes in bias voltage can now be considered. Differentiating Eq. (4) yields

$$\frac{\partial A_V}{\partial V_B} = \frac{qR_L}{2kT} \cdot \frac{I_S}{V_B}$$

Differentiation of Eq. (6) yields

$$\frac{\partial I_S}{\partial V_B} = \frac{1}{R_S} - \frac{1}{R_S} \cdot \frac{\partial V_{BE}}{\partial I_S}$$

where

$$\frac{\partial V_{BE}}{\partial I_S} = \frac{kT}{qI_S} \cong 0.05 \, R_S$$

Hence,

$$\frac{\partial I_S}{\partial V_B} = \frac{1}{R_S}$$

and

$$\frac{\partial A_V}{\partial V_B} = \frac{qR_L}{2kT R_S}$$

From Eqs. (4) and (6), we can write

$$\frac{\partial A_V}{\partial V_B} = \frac{A_{VO}}{I_S R_S} = \frac{A_{VO}}{V_B - V_{BE}}$$

Using the same arguments that would have to be applied in going to Eq. (20),

$$\Delta A_V = \frac{A_{VO} \, \Delta V_B}{V_B - V_{BE}} \tag{22}$$

which gives the change in voltage gain for a change in bias voltage.

The total deviation in gain from the design center value is obtained by combining Eqs. (17), (21), and (22), which results in

$$\Delta A_V = \frac{A_{VO} \, \Delta V_B}{V_B - V_{BE}} - \frac{A_{VO}^2 R_E}{R_L} - \frac{A_{VO}}{h_{FE}}\left(\frac{R_B}{R_S} + 2\right)$$

or

$$\frac{\Delta A_V}{A_{VO}} = \frac{\Delta V_B}{V_B - V_{BE}} - \frac{A_{VO} R_E}{R_L} - \frac{1}{h_{FE}}\left(\frac{R_B}{R_S} + 2\right) \tag{23}$$

If $R_B < R_S$, this becomes

$$\frac{\Delta A_V}{A_{VO}} = \frac{\Delta V_B}{V_B - V_{BE}} - \frac{A_{VO} R_E}{R_L} - \frac{2}{h_{FE}} \tag{24}$$

The differential amplifier designs described in the text operate at approximately 1 mA collector current. At this current, a transistor with a very low emitter contact and base spreading resistance is needed. In addition, since high-frequency response is of major concern, the collector-base capacitance must be small. A device that satifies these requirements is the Fairchild 2N3302 (or 2N3729 matched pair). The resistive component of transconductance is so small as to be difficult to measure and its temperature coefficient is well behaved. Since it can be compensated for in the initial gain setting it can be neglected completely in design.

The current gain term, however, cannot be disposed of so easily for operation over the full temperature range. From Eq. (24) a current gain of 20 (which would be a reasonable minimum at -55°C) gives a gain error of 10 percent. Therefore, in a production situation where units were not selected, a 10-percent gain error could be encountered at the low temperature extreme even though the room temperature gain was set to the desired value.

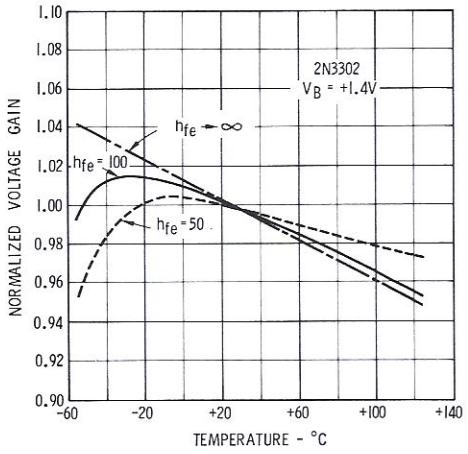

Fig. 2a. Voltage gain of the compensated differential amplifier as a function of ambient temperature for various room temperature current gains.

Increasing the bias voltage, V_B, will give the gain a negative temperature coefficient. This can be used to partially compensate for the gain variation due to low gain fall-off at low temperature. This compensation will not be exact, however, since the h_{FE} term does not give a linear variation of gain with temperature. Experimental data showing the result of this second-order compensation are given in Fig. 2A. The optimum bias voltage was empirically determined to be 1.4 V for -55°C to +125°C operation. This gives a gain stability of ± 5 percent over the full temperature range for all units with a room temperature h_{FE} greater than 50. For limited temperature range operation (0-70°C), the optimum bias voltage is 1.3 V, and a 1-percent gain stability can be realized.

As can be seen from the first term of Eq. (24), the gain is affected by changes in bias voltage. The magnitude of this term can be estimated by using the typical emitter-base voltages given in Fig. 3A. For a bias voltage of 1.4 V, the change in gain for a 1-percent change in bias voltage will be 1.9 percent at room temperature, 2.3 percent at -55°C, and 1.5 percent at +125°C. The temperature coefficient of the gain, however, will not be noticeably affected by changes of this magnitude.

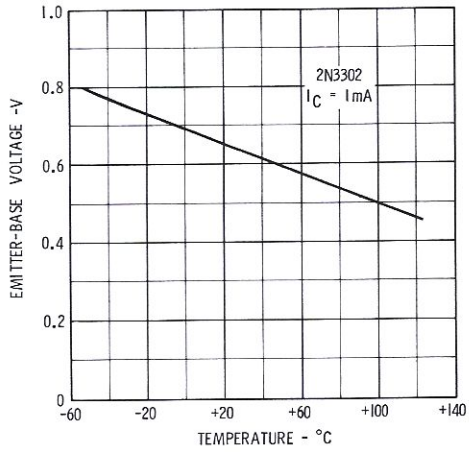

Fig. 3a. Emitter-base voltage as a function of temperature for a typical Fairchild 2N3302 operating at 1 mA collector current.

Only one bias supply is needed for the entire memory, but relative precision and a very low internal impedance is required. A Fairchild μA 702A operational amplifier and a compensated voltage reference can be used to supply this voltage.

The analysis leading to Eq. (11) showed that the gain compensation was independent of the magnitude of V_{BE}; however, the magnitude of the gain is not. Using a derivation similar to that for Eq. (22), it can be shown that

$$\frac{\Delta A_V}{A_{VO}} = - \frac{\Delta V_{BE}}{V_B - V_{BE}} \qquad (25)$$

The production variation of V_{BE} for a particular transistor will normally be less than ± 50 mV (the variation

within a lot is substantially less than this). Hence, using Eq. (25) and the value for V_{BE} given in Fig. 2A, one can find a variation of ± 6.7 percent due to differences in emitter-base voltage among different current-source transistors. This can be adjusted out, as can all other initial errors, without affecting gain compensation by changing the current-source emitter resistor, R_S.